A Dual Bias-Feed Circuit Design for SiGe HBT Low-Noise Linear Amplifier

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***Abstract*—An SiGe HBT low-noise amplifier (LNA) with a novel diode/resistor dual base bias-feed circuit is described. The dual bias-feed circuit extends $P1$ dB without degradation of the noise figure (NF). In the small-signal region, a conventional resistor bias-feed circuit is a dominant base current source and, in the large-signal region, the diode turns on and the diode bias-feed circuit supplies the base current like a voltage source, which allows higher output power and linearity. In this paper, the operation principle of the dual bias-feed circuit is explained by using a virtual current source model, which indicates the increase of base current of the HBT in a large-signal region. The design method is also described for the idle current of the diode bias-feed circuit in a small-signal region from the points-of-view of NF and $P1$ dB. The effectiveness of the dual bias-feed circuit is evaluated by simulation and measurement. The fabricated 2-GHz-band dual bias-feed LNA has the $P1$ dB improvement of 5 dB and no degradation NF compared with the conventional resistor bias-feed LNA.**

***Index Terms*—Microwave bipolar transistor, monolithic microwave integrated circuit (MMIC) amplifiers, silicon, UHF amplifiers.**

I. Introduction

FOR LOW-NOISE amplifiers (LNAs) used in mobile communication terminals, small size, low noise performance, and low dc current operation have been required [1]–[3]. Recently, high-saturated RF power and linearity have been also desired [1] for the LNAs used for frequency-division duplexing (FDD) systems, such as W-CDMA [4]. For the size reduction of the RF section, system chips using Si technologies have been reported [5]–[7]. The development of an SiGe process [8]–[11], having higher RF performance than conventional Si processes, has allowed us to design lower noise and lower dc current drive LNAs. In the case of an SiGe transceiver system chip for an FDD system, the leakage of the transmit (Tx) signal to the receiver section [12] becomes a serious problem due to the low isolation on a low-resistivity Si substrate. To avoid the interference from the leakage of the Tx signal, high saturated power and linearity are needed for the LNA.

In the case of bipolar junction transistor (BJT) LNAs, including the SiGe HBT LNA, the design of the base bias circuit is a key issue to obtain high $P1$ dB [13]. Since the transistor size is large enough to achieve low noise figure (NF) and the dc current is limited [1], the transistor should be driven near the pinchoff bias point. Therefore, an inductor bias feed and a constant voltage source have been used for the base bias circuit to obtain high $P1$ dB and linearity [14]. From the viewpoint of size reduction, the inductor bias-feed circuit needs an area consumptive off- or on-chip inductor, and the use of an on-chip resistor bias feed instead of an inductor bias feed is preferable [1], [11].

In this paper, the operation principle and design method of the dual bias-feed-type base bias circuit for the linear LNA [15] has been described. The bias circuit consists of two different bias-feed circuits connected in parallel. One is a conventional on-chip resistor bias-feed circuit, and the other is an on-chip diode bias-feed circuit. The diode bias-feed circuit is regarded as an open circuit in the small-signal region and a voltage source in the large-signal region. The operation principle of the dual bias-feed circuit is described in Section II by using a virtual current source model, which indicates the increase of base current of the HBT in the large-signal region. The design of the idle current supplied from the diode bias-feed circuit is described in Section III from the points-of-view of the NF and $P1$ dB. The idle current is designed to satisfy the desired NF and saturation power. The measured results of the fabricated LNA are described in Section IV.

II. Operation Principle of Dual Bias-Feed Circuit

An HBT used in an LNA should have a large emitter area to achieve low NF and should be driven near the pinchoff bias point to reduce supplied dc current. Therefore, the use of a constant voltage source and inductor bias-feed circuit is preferable to obtain low-NF, high-$P1$ dB, and linearity. An on-chip inductor bias-feed circuit causes loss and needs a large area on an integrated circuit (IC) chip. On the other hand, an off-chip inductor causes the increase of the number of external components. Therefore, on-chip resistor bias-feed LNAs having low $P1$ dB and linearity have been widely employed for wireless terminals. To address these problems, a dual bias-feed circuit, which has two different bias-feed circuits connected in parallel, is proposed. One is a conventional on-chip resistor bias-feed circuit, and the other is an on-chip diode bias-feed circuit. These two different types bias circuits can be easily integrated in a very small area on the IC chip, and allow higher $P1$ dB and linearity than a conventional resistor bias-feed LNA.

Fig. 1 shows three types of bias circuit models for dc component analysis. Fig. 1(a) is an inductor bias feed, Fig. 1(b) is

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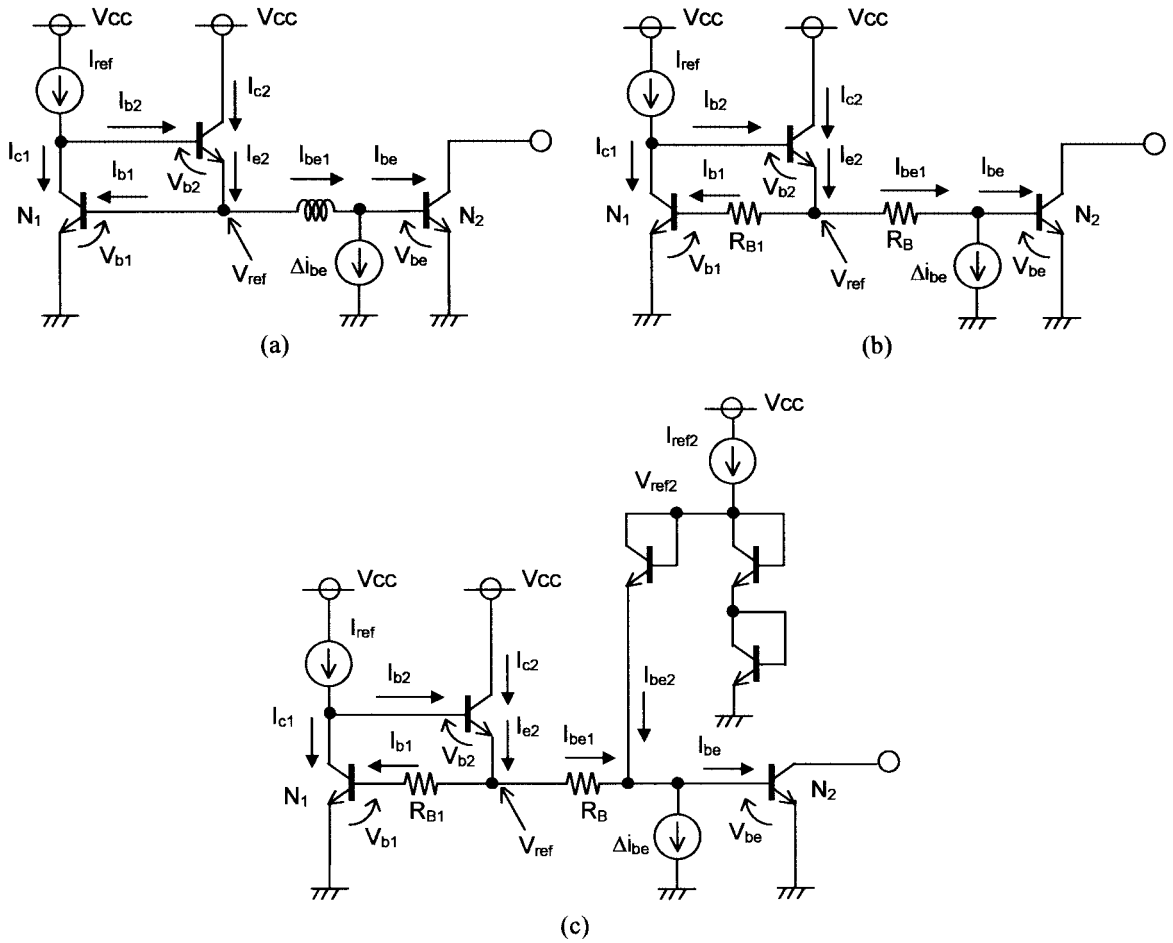

Fig. 1. Three types of bias circuit models for dc component analysis. (a) Inductor bias feed. (b) Resistor bias feed. (c) Dual bias feed. N_1 and N_2 indicate the emitter area factor of each transistor. The virtual current model ibe shows the increase of base current in the large-signal region.

a resistor bias feed, and Fig. 1(c) is a dual bias feed. A virtual current source Δi_{be} is added to each cases, which indicates the increase of base current in the large-signal region. To simplify the analysis, it is assumed that all transistor in the bias circuits have same forward current gain of h_{FE} and saturation current of I_S. Ratio of transistor size used in the bias circuit and LNA is $N_1 : N_2$.

A. Inductor Bias Feed

In the case of inductor bias feed, shown in Fig. 1(a), $V_{\rm ref}$ can be expressed as

$$V_{\rm ref} = V_{b1} = V_T \ln\left(\frac{I_{c1}}{I_S}\right) \tag{1}$$

where V_T indicates thermal voltage, which is equal to kT/q, 26 mV in room temperature. In Fig. 1(a), the current flows at each node are expressed as

$$I_{c1} = I_{\rm ref} - I_{b2} \tag{2a}$$
$$I_{b2} = I_{e2}/(h_{FE}+1) \tag{2b}$$
$$I_{e2} = I_{b1} + I_{be} + \Delta i_{be} \tag{2c}$$
$$I_{b1} = I_{c1}/h_{FE}. \tag{2d}$$

By using (1) and (2a)–(2d), $V_{\rm ref}$ can be written as

$$\begin{aligned} V_{\rm ref} &= V_T \ln\left\{\frac{1}{I_S}\left[I_{\rm ref} - \frac{I_{c1}}{h_{FE}(h_{FE}+1)} \cdot\left(1+\frac{N_2}{N_1}+\frac{\Delta i_{be}}{I_{b1}}\right)\right]\right\} \\ &= V_T \ln\left\{\frac{1}{I_S}\left[I_{\rm ref} - \frac{I_S \exp(V_{\rm ref}/V_T)}{h_{FE}(h_{FE}+1)} \cdot\left(1+\frac{N_2}{N_1}+\frac{\Delta i_{be}}{I_{b1}}\right)\right]\right\} \end{aligned} \tag{3}$$

where

$$I_{be} = \frac{N_2}{N_1} I_{b1}. \tag{4}$$

Dividing both sides of (3) by V_T, it becomes

$$\frac{V_{\rm ref}}{V_T} = \ln\left\{\frac{1}{I_S}\left[I_{\rm ref} - \frac{I_S \exp(V_{\rm ref}/V_T)}{h_{FE}(h_{FE}+1)} \cdot\left(1+\frac{N_2}{N_1}+\frac{h_{FE}\Delta i_{be}}{I_S \exp(V_{\rm ref}/V_T)}\right)\right]\right\}. \tag{5}$$

Equation (5) is then transformed into

$$I_S \exp\left(\frac{V_{\rm ref}}{V_T}\right) = I_{\rm ref} - \frac{I_S \exp(V_{\rm ref}/V_T)}{h_{FE}(h_{FE}+1)}\left(1+\frac{N_2}{N_1}\right) \frac{\Delta i_{be}}{(h_{FE}+1)}. \tag{6}$$

By arranging the exponential terms, (6) is rewritten as

$$\left[1+\frac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}\right]\cdot I_S\exp\left(\frac{V_{\rm ref}}{V_T}\right)=I_{\rm ref}-\frac{\Delta i_{be}}{(h_{FE}+1)}. \tag{7}$$

From (7), $V_{\rm ref}$ can be expressed as

$$V_{\rm ref} =V_T\ln\left\{\frac{1}{I_S}\left[\frac{I_{\rm ref}}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}-\frac{\Delta i_{be}/(h_{FE}+1)}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}\right]\right\}. \tag{8}$$

Since an inductor is used for the bias feed, the base voltage is equal to $V_{\rm ref}$ as follows:

$$V_{be}=V_{\rm ref}. \tag{9}$$

By substituting (8) into (9), the base voltage V_{be} can be obtained as

$$\begin{aligned}V_{be} &=V_T\ln\left\{\frac{1}{I_S}\left[\frac{I_{\rm ref}}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}-\frac{\Delta i_{be}/(h_{FE}+1)}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}\right]\right\}\\ &\approx V_T\ln\left\{\frac{1}{I_S}\left[\frac{I_{\rm ref}}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}\right]\right\}.\end{aligned} \tag{10}$$

where

$$\frac{\Delta i_{be}}{h_{FE}+1}\ll 1. \tag{11}$$

Equation (10) shows that the base voltage is independent of Δi_{be} and does not change in the large-signal region. Therefore, the inductor bias-feed LNA can obtain high saturation power and linearity.

B. Resistor Bias Feed

In the case of resistor bias feed, shown in Fig. 1(b), $V_{\rm ref}$ can be expressed as

$$V_{\rm ref}=V_{b1}+I_{b1}R_{B1} \tag{12}$$

and the base voltage V_{be} can be expressed as

$$V_{be}=V_{\rm ref}-(I_{be}+\Delta i_{be})R_B. \tag{13}$$

By substituting (4) and (12) into (13), V_{be} is rewritten as

$$\begin{aligned}V_{be} &=V_{b1}+I_{b1}R_{B1}-(I_{be}+\Delta i_{be})R_B\\ &=V_{b1}+I_{b1}\left(R_{B1}-\frac{N_2}{N_1}R_B\right)-R_B\Delta i_{be}\\ &=V_{b1}+\frac{I_S}{h_{FE}}\exp\left(\frac{V_{b1}}{V_T}\right)\left(R_{B1}-\frac{N_2}{N_1}R_B\right)-R_B\Delta i_{be}.\end{aligned} \tag{14}$$

The base voltage V_{b1} of the resistor bias feed is equal to V_{be} of the inductor bias feed. From (10), V_{b1} can be expressed as

$$V_{b1}\approx V_T\ln\left\{\frac{1}{I_S}\left[\frac{I_{\rm ref}}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}\right]\right\}. \tag{15}$$

By substituting (15) into (14), V_{be} can be obtained as

$$V_{be}=V_T\ln\left\{\frac{1}{I_S}\left[\frac{I_{\rm ref}}{1+\dfrac{1+N_2/N_1}{h_{FE}(h_{FE}+1)}}\right]\right\}-R_B\Delta i_{be} \tag{16}$$

where

$$R_B=\frac{N_1}{N_2}R_{B1}. \tag{17}$$

Equation (16) shows that the base voltage V_{be} is dependent on the increase of base current Δi_{be}, and V_{be} decreases as Δi_{be} increases according to the increase of input RF power. Therefore, the resistor bias-feed LNA has lower saturation power and linearity than the inductor bias-feed LNA.

C. Dual Bias Feed

In the case of the dual bias feed, shown in Fig. 1(c), $V_{\rm ref}$ can be expressed by (12). The base voltage V_{be} then becomes

$$\begin{aligned}V_{be} &=V_{\rm ref}-I_{be1}R_B\\ &=V_{b1}+I_{b1}R_{B1}-I_{be1}R_B\\ &=V_{b1}+I_{b1}R_{B1}-(I_{be}-I_{be2}+\Delta i_{be})R_B.\end{aligned} \tag{18}$$

To avoid noise degradation, I_{be2} is set to negligible small value compared with I_{be1} in the small —signal region, i.e., $\Delta i_{be}=0$. Therefore, the relationship between I_{b1} and I_{be} can be assumed as

$$I_{be}\approx\frac{N_2}{N_1}I_{b1}. \tag{19}$$

By substituting (19) into (18), V_{be} is rewritten as

$$\begin{aligned}V_{be} &=V_{b1}+\left(I_{b1}R_{B1}-\frac{N_2}{N_1}I_{b1}R_B\right)-(\Delta i_{be}-I_{be2})R_B\\ &=V_{b1}-(\Delta i_{be}-I_{be2})R_B.\end{aligned} \tag{20}$$

The current from diode bias-feed circuit I_{be2} is written as

$$\begin{aligned}I_{be2} &=\frac{h_{FE}}{1+h_{FE}}I_S\exp\left(\frac{V_{\rm ref2}-V_{be}}{V_T}\right)\\ &=\frac{h_{FE}}{1+h_{FE}}I_S\exp(\alpha)\exp(\beta)\exp(\gamma)\end{aligned} \tag{21}$$

where

$$\alpha=\frac{V_{\rm ref2}-V_{b1}}{V_T}$$
$$\beta=\frac{\Delta i_{be}R_B}{V_T}$$
$$\gamma=\frac{-I_{be2}R_B}{V_T}. \tag{22}$$

Since the base voltage V_{b1} of dual bias feed is almost equal to that of the resistor bias feed, it is possible to substitute (15) into (21). By differentiating I_{be2} with respect to Δi_{be}

$$\begin{aligned}\frac{\partial I_{be2}}{\partial \Delta i_{be}} &= \frac{h_{FE}}{1+h_{FE}} I_S \left\{ \frac{\partial V_{b1}}{\partial \Delta i_{be}} + \frac{R_B}{V_T} - \frac{\partial I_{be2}}{\partial \Delta i_{be}} \frac{R_B}{V_T} \right\} \\ &\quad \cdot \exp(\alpha)\exp(\beta)\exp(\gamma) \\ &= \frac{h_{FE}}{1+h_{FE}} I_S \left\{ \frac{R_B}{V_T} - \frac{\partial I_{be2}}{\partial \Delta i_{be}} \frac{R_B}{V_T} \right\} \\ &\quad \cdot \exp(\alpha)\exp(\beta)\exp(\gamma). \end{aligned} \tag{23}$$

By arranging $\partial I_{be2}/\partial \Delta i_{be}$, (23) is rewritten as

$$\begin{aligned}\frac{\partial I_{be2}}{\partial \Delta i_{be}} &= \frac{\dfrac{h_{FE}}{1+h_{FE}} \dfrac{R_B}{V_T} I_S \exp(\alpha)\exp(\beta)\exp(\gamma)}{1 + \dfrac{h_{FE}}{1+h_{FE}} \dfrac{R_B}{V_T} I_S \exp(\alpha)\exp(\beta)\exp(\gamma)} \\ &= \frac{\dfrac{R_B}{V_T} I_{be2}}{1 + \dfrac{R_B}{V_T} I_{be2}} = 1 - \frac{1}{1 + \dfrac{R_B}{V_T} I_{be2}}. \end{aligned} \tag{24}$$

In the large-signal region, Δi_{be} become large, and then I_{be2} can be expressed as

$$I_{be2} \gg \frac{V_T}{R_B}. \tag{25}$$

Equation (24) then becomes

$$\frac{\partial I_{be2}}{\partial \Delta i_{be}} = 1 \tag{26}$$

and it shows that most of the increasing base current is supplied from the diode bias-feed circuit, and the base voltage is constant in the large-signal region. As a result, the dual bias-feed LNA can achieve higher saturation power and linearity than the resistor bias-feed LNA.

While the base current of the LNA transistor is mainly supplied from the current-mirror circuit in the small-signal region because the current from the reference diode is relatively small, the base current is provided by both the current-mirror circuit and the reference diode in the large-signal region. As the RF signal increases, the average V_{be} of the LNA transistor tends to decrease due to an increased voltage drop on R_B. However, a drop on V_{be} will increase the voltage drop across the reference diode and, therefore, increase I_{be2}. This will, in turn, compensate or boost the voltage drop of the LNA transistor.

In the large-signal region, the reference diode could be turned on and off (or strongly on and weakly on) by the RF signal. A value of the average V_{be} of the LNA transistors depends upon charging and discharging time constants of its base current paths. It could be even larger than the quiescent V_{be}. The circuit technique is effectively a bias-boosting technique.

III. Design

A. Design of Diode Bias-Feed Circuit Current

For the dual bias-feed LNA, the design of the diode bias-feed circuit current is an important issue to achieve both of the desired NF and $P1$ dB. To obtain high $P1$ dB, the current of the dual bias-feed circuit I_{be2} should satisfy (25). However, there is a limit for I_{be2} because I_{be2} is related to the impedance of the diode bias-feed circuit and a large I_{be2} causes the degradation of noise performance of the LNA.

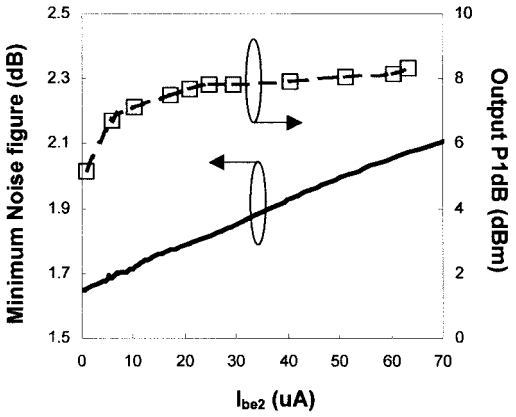

Fig. 2. Simulated idle current of I_{be2} versus minimum NF and output $P1$-dB characteristics of the LNA using a dual bias-feed circuit.

Fig. 2 shows the simulated idle current of I_{be2} versus the minimum NF and output $P1$ dB of the dual bias-feed LNA. In the simulation, the total base current I_{be} of the HBT is set to approximately 70 μA. The resistor R_B of 3 kΩ and R_{B1} of 30 kΩ are used in consideration of the area consumption of the fabricated IC. Thus, $V_T/R_B = 9$ μA. As shown in Fig. 2, at the region of $I_{be2} < V_T/R_B$, a low-noise characteristic can be achieved, however, the $P1$ dB is relatively low. At the region of $I_{be2} > V_T/R_B$, the $P1$ dB is improved, but the NF is degraded. To achieve both low-noise and high $P1$ dB performances, idle current of I_{be2} is designed as 17 μA.

B. Design of LNA

To evaluate the effectiveness of the dual bias-feed LNA, simulation is carried out for the three types of LNA having different base bias circuits. The circuit configurations of those LNAs are already shown in Fig. 1. The bias-feed inductor of $L_B = 8$ nH, resistor of $R_B = 3$ kΩ, and $R_{B1} = 30$ kΩ are used in simulation. Figs. 3 and 4 show the simulated base voltage V_{be} and the base current I_{be} dependences on the input power for the LNAs.

To achieve low noise and low dc power operation, the HBT is usually driven near the pinchoff bias point. Therefore, the inductor bias-feed circuit, shown in Fig. 1(a), is preferable to obtain low-noise performance, high $P1$ dB, and linearity. By using an inductor as the bias feed, as shown in Figs. 3(a) and 4(a), V_{be} becomes constant and I_{be} can increase in the large-signal region to extend its output power. The resistor bias-feed circuit, shown in Fig. 1(b), has been widely used as the conventional base bias circuit. To avoid NF degradation due to the resistor bias-feed circuit, the value of the resistor is usually designed as several kiloohms. In the large-signal region, since the bias point of the HBT is near pinchoff, I_{be} should be increased; however, voltage drop due to the feed resistor has occurred. V_{be} is then dropped, and the increment of I_{be} have to be limited, as shown in Figs. 3(b) and 4(b). In the case of the dual bias-feed LNA, shown in Fig. 1(c), the diode bias-feed circuit is added to the

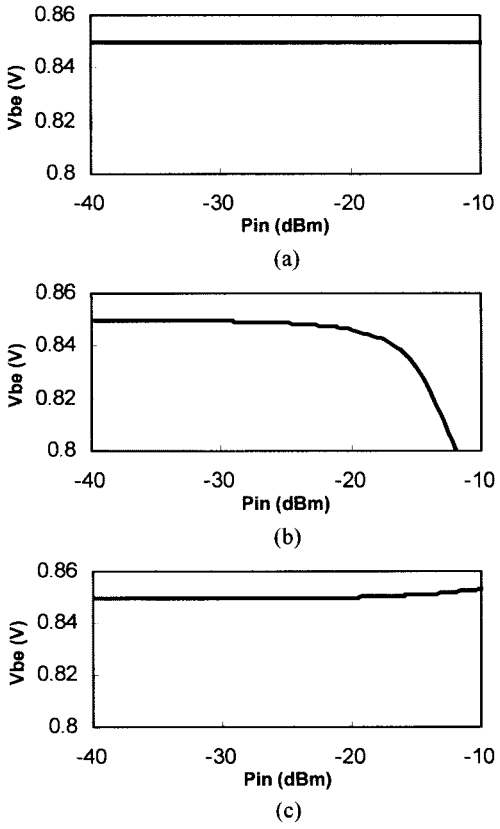

Fig. 3. Simulated RF input power pin versus base voltage V_{be}. (a) Inductor bias feed. (b) Resistor bias feed. (c) Dual bias feed.

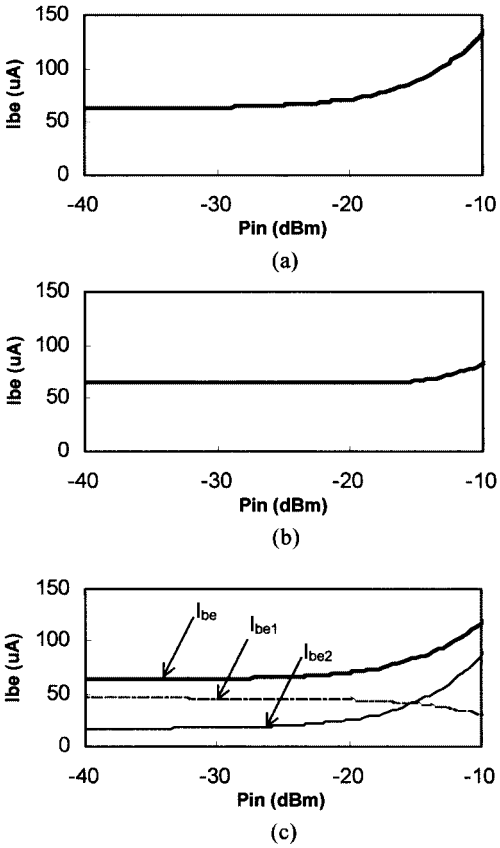

Fig. 4. Simulated RF input power pin versus base current I_{be}. (a) Inductor bias feed. (b) Resistor bias feed. (c) Dual bias feed.

conventional resistor bias-feed LNA, and it avoids a V_{be} drop in the large-signal region. As shown in Section III-A, the idle current I_{be2} supplied from the diode bias feed has been designed as 17 μA to reduce degradation of the NF and to obtain higher $P1$ dB. V_{be} and I_{be} characteristics, shown in Figs. 3(c) and 4(c), are similar to those of the inductor bias-feed LNA.

Fig. 5 shows the simulated transfer characteristics of LNAs having different base bias circuits. The resistor bias-feed LNA has the lowest $P1$ dB, and the proposed dual bias-feed LNA has improved performance from the resistor feed LNA.

For W-CDMA utilization, the interference of Tx power leakage in the LNA becomes a problem. To investigate this effect, NF degradation due to the Tx power leakage is simulated. Fig. 6 shows the simulated NF degradation and Vbe of LNAs versus the Tx power leakage. As the Tx power leakage increases, NF degradation has occurred in every bias-feed types of LNAs. It is clear that the inductor bias-feed LNA shows the best performance. Comparing the dual bias-feed LNA with the resistor bias-feed LNA, the dual bias-feed LNA shows relatively stable NF characteristic at a high Tx power leakage region (over -20 dBm). At this region, the resistor bias-feed LNA shows a rapid V_{be} drop and it results in abrupt NF degradation.

Simulated characteristics of the resistor bias-feed and dual bias-feed LNAs at a typical condition (temperature of 25 °C and supply voltage Vcc of 3 V) are summarized in Table I. Simulation results shows that the dual bias-feed LNA allows over 4-dB improvement of $P1$ dB with comparable gain, NF, and

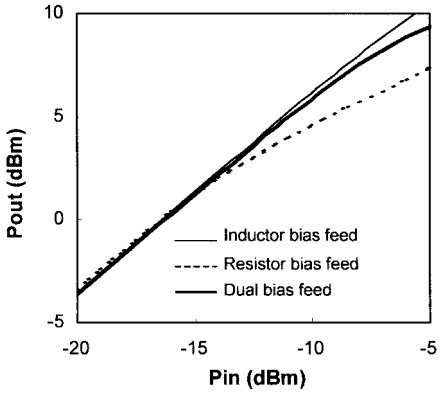

Fig. 5. Simulated transfer characteristics of LNAs using three types of base bias-feed circuits. $I_{ce} = 5$ mA and $V_{be} = 0.85$ V for dc condition, respectively. The frequency of the input signal is 2.1 GHz.

supplied dc current. The simulated performance deviations of the resistor bias-feed and dual bias-feed LNAs over temperature and Vcc are shown in Table II. The performance deviations of the proposed dual bias-feed LNA are also comparable to the conventional resistor bias-feed LNA.

IV. Implementation and Measurement

Based on the design shown in Section III, the LNA having a dual bias-feed circuit is fabricated. For comparison, the LNA having a conventional resistor bias-feed circuit is also fabricated. Schematic diagrams of those two LNAs are shown

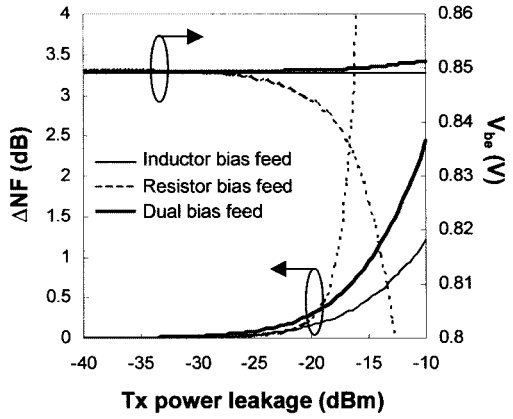

Fig. 6. Simulated NF degradation and V_{be} of LNAs versus the Tx power leakage.

TABLE I
SUMMARY OF SIMULATED PERFORMANCES OF LNAs (@2.1 GHz, TEMPERATURE = 25 °C AND Vcc = 3 V)

	Resistor Bias Feed	Dual Bias Feed
I_{TOTAL} (mA)	5.8	6.1
I_{be} (μA)	63.7	63.7
I_{be2} (μA)	-	17
Gain (dB)	16.7	16.5
NF (dB)	1.5	1.5
OP1dB (dBm)	+2.7	+7.5
Tx power leakage for 1dB NF degradation (dBm)	-17.9	-14.7

TABLE II
SIMULATED PERFORMANCE DEVIATIONS OF LNAs OVER TEMPERATURE AND SUPPLY VOLTAGE (@2.1 GHz)

		Temperature (°C)		Vcc (V)	
		-20	80	2.85	3.15
Resistor Bias Feed	ΔGain (dB)	0.2	-0.2	0.0	0.1
	ΔNF(dB)	-0.2	0.2	-0.1	0.1
	ΔOP_{1dB}(dB)	-0.8	0.8	-1.1	1.0
Dual Bias Feed	ΔGain(dB)	0.1	-0.2	-0.1	0.0
	ΔNF(dB)	-0.2	0.2	-0.1	0.1
	ΔOP_{1dB}(dB)	0.1	-0.2	-0.1	0.5

in Fig. 7. Fig. 7(a) shows the conventional resistor bias-feed LNA and Fig. 7(b) shows the dual bias-feed LNA. Both LNAs need external circuit components, i.e., matching circuits, collector bias-feed circuits, and reference resistors. The external matching network is shown in Fig. 8. The die photograph of the fabricated dual bias-feed LNA is shown in Fig. 9. The chip area of the LNA is 1.0 mm × 0.6 mm, and the area of the additional diode feed circuit is 97 μm × 65 μm.

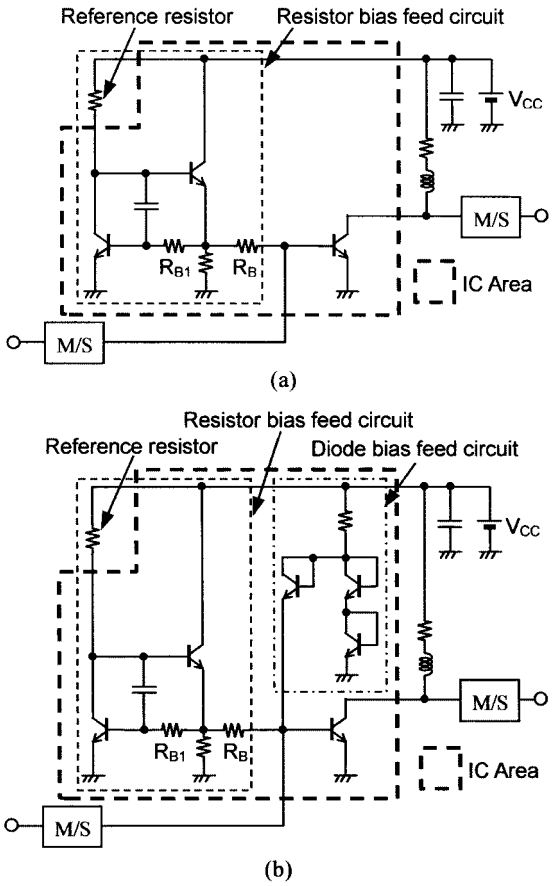

Fig. 7. Schematic diagrams of LNAs fabricated in the SiGe process. (a) Resistor bias feed. (b) Dual bias feed. IC areas are indicated by the dotted line.

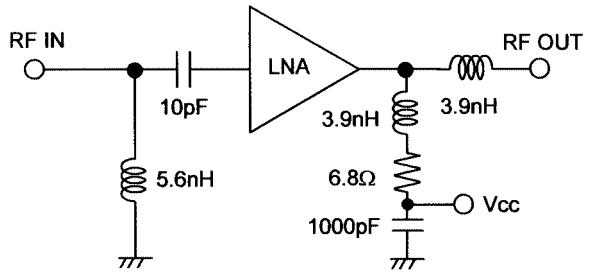

Fig. 8. External matching network of the LNAs. The same matching circuit is used for both LNAs.

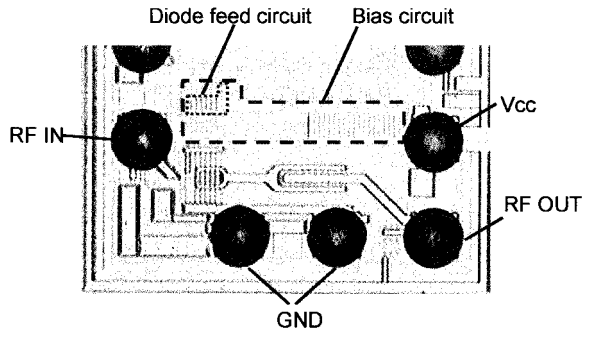

Fig. 9. Die photograph of the fabricated dual bias-feed LNA. The chip area is 1.0 mm × 0.6 mm.

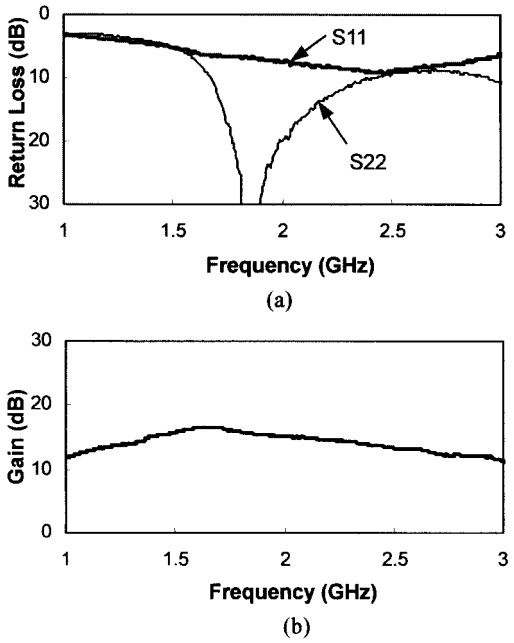

Fig. 10. Measured small-signal characteristics of the dual bias-feed LNA. (a) Return loss. (b) Gain.

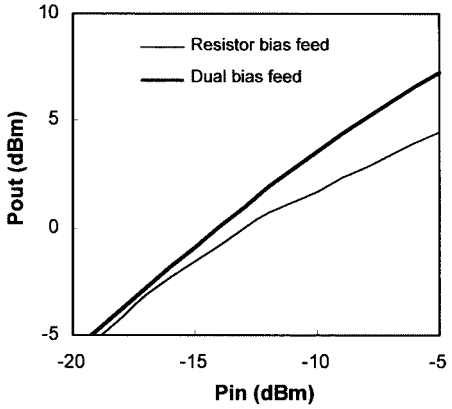

Fig. 11. Measured transfer characteristics of LNAs using two types of base feed circuit. The frequency of the input signal is 2.1 GHz.

Measured small-signal characteristics of the dual bias-feed LNA are shown in Fig. 10. Since the input port is matched to obtain a low NF, the input return loss is 8.2 dB, whereas the output return loss is 15.1 dB. Small-signal gain of 14.8 dB is obtained with a supplied voltage of 3 V and a total current of 6.1 mA. Fig. 11 shows the measured transfer characteristics of the LNAs having different base bias-feed circuits. The output $P1$ dB of the dual bias-feed LNA is $+4.5$ dBm and is 5.3 dB higher than that of the conventional resistor bias-feed LNA. Fig. 12 shows the measured third-order intermodulation (IM3) characteristics of the LNAs. The input third intercept point (IIP3) of the dual bias-feed LNA is $+0.2$ dBm and is 6.1 dB higher than that of the resistor bias-feed LNA. The measured results of both LNAs are summarized in Table III. The dual bias-feed LNA allows more than 5-dB improvement of both $P1$ dB and IIP3 with comparable gain, NF, and supplied dc current.

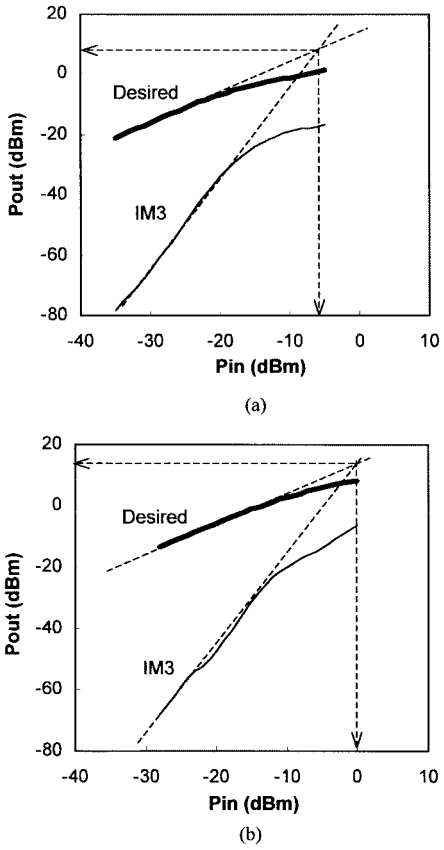

Fig. 12. Measured two-tone transfer characteristics of LNAs using two types of base bias-feed circuit. (a) Resistor bias feed. (b) Dual bias feed.

TABLE III
SUMMARY OF MEASURED PERFORMANCES OF LNAs (@2.1 GHz)

		Resistor Bias Feed	Dual Bias Feed
I_{TOTAL} (mA)		5.9	6.1
Gain (dB)		14.2	14.8
NF (dB)		2.2	2.0
Return Loss(dB)	IN	19	8.2
	OUT	9.9	15.1
OP1dB (dBm)		-0.8	+4.5
IIP3 (dBm)		-5.9	+0.2

V. CONCLUSIONS

A novel diode/resistor dual base bias-feed LNA has been discussed. The operation principle and the design method of the dual base bias-feed circuit has been described. The derived equations shown in Section II indicates that the dual bias-feed circuit operates like a conventional resistor bias-feed circuit in the small-signal region; therefore, low noise performance can be obtained. It also operates like a constant-voltage source in the large-signal region; therefore, high $P1$ dB and IP3 can be achieved. Since this bias-feed circuit does not need any area consumptive inductors, a compact on-chip base bias circuit can be realized. The design method of base bias-feed currents to achieve both low noise and high $P1$ dB have also been

described. Based on this design method, an SiGe HBT LNA has been designed and fabricated. The fabricated dual bias-feed SiGe HBT LNA performs higher $P1$ dB and IP3 than that of the conventional resistor bias-feed LNA.

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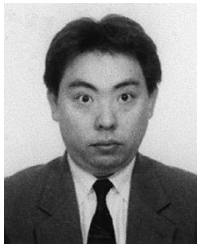

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